

AMENDMENT

The Commissioner is hereby authorized to charge payment of any additional fees involved with added Claims and the like to Deposit Account No. 19-0033.

IN THE DRAWINGS

One replacement sheet marked in red for corrections for Fig. 1 is submitted for approval. Correction is made to one erroneously labeled reference numeral. No new matter added.

IN THE SPECIFICATION

On page 15, please replace the second paragraph with the following rewritten paragraph:

Next, floating gate oxide layer (160) is grown over the substrate, as shown in Fig. 2c. Subsequently, a first conductive layer (170)-a polysilicon- later to be formed into a floating gate, is deposited over the gate oxide layer. Polysilicon is formed through methods including but not limited to Low Pressure Chemical Vapor Deposition

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(LPCVD) methods, Chemical Vapor Deposition (CVD) methods and Physical Vapor Deposition (PVD) sputtering methods employing suitable silicon source materials. The floating gates are next defined by patterning a photoresist layer over the polysilicon layer and the floating gates formed by etching the first polysilicon layer exposed through the patterns in the photoresist layer, after which the photoresist layer is removed.

On page 19, please replace the second paragraph with the following rewritten paragraph:

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An interpoly oxide (280) is next formed over the contours of the conformal floating gate as shown in Fig. 3c. It is preferred that the interpoly oxide comprises oxide/nitride/oxide (ONO) formed through methods known in the art. Then, a second conductive layer (290), a polysilicon, is formed over the interpoly oxide as shown both in the top view of the substrate in Fig. 3d, as well as the cross-sectional view, Fig. 3e. A third photoresist layer (not shown) is then used to form the control gate and word line (290) shown in Fig. 3e. A still another fourth photoresist layer (not shown) is used to define the self-aligned source (SAS) to form a common source line (200)